Remarks/Arguments:

Claims 1-18 are pending. Claims 1-18 stand rejected.

Section 102/103 Rejections:

Claims 1-18 have been rejected as being anticipated by Gowda, or as being obvious in view of Gowda. Applicants respectfully submit that this rejection is overcome for the reasons set forth below.

Amended claim 1 now includes features which are not suggested by the cited reference, namely:

- the sample-and-hold circuit from the first bank is selectively connected to a row of the array for sampling a succession of reset voltages **only** from corresponding columns of **the selected row**, and
- the sample-and-hold circuit from the second bank of the array is selectively connected to **the same row** of the array for sampling a succession of integrated voltages **only** from the corresponding columns of **the same row.**

Basis for amended claim 1 may be found, for example, at paragraph 26 of page 5 in the specification and in FIG. 4. As described, sample and hold circuits 330 include two banks 331 and 332. Each bank 331 or 332 includes one sample and hold circuit per column of the pixel sensor array. Accordingly, for each column of array 110, sample and hold circuits 330 can simultaneously hold two analog voltage levels (one in each bank) corresponding to the column line voltage at different times.

As best shown in FIG. 4, while reading out row-0 of array 110, the first bank is connected to read out the reset voltages of row-0, and the second bank is connected to read out the integrated voltages of row-0. Similarly, when reading out row-1 of the array, the first bank is connected to read out the reset voltages of row-1, and the second bank is connected to read out the integrated voltages of row-1. Accordingly, there is one channel for reading the reset voltage in each column of a specific row, and there is another channel for simultaneously reading the integrated voltage in each column of the specific row.

Gowda, on the other hand, discloses an image sensor for correlated double sampling. As shown in FIG. 3, ADC 40_1 samples the output signals provided by pixel 30 of column C_1. Similarly, ADC 40_2 samples the output signals provided by pixel 30 of column C_2. Accordingly, a single ADC is provided to sample each pixel of a particular column. Gowda does **not** suggest selectively **connecting a first bank to a row of the array** for sampling a succession of reset voltages **only from corresponding columns of the selected row**. Furthermore, Gowda does **not** suggest selectively **connecting a second bank to the same row of the array** for

sampling a succession of integrated voltages **only from the corresponding columns of the same selective row.**

When performing correlated double sampling, Gowda first samples the reset voltages from each column and then samples the integrated voltages from each column. However, Gowda has no capability for separating the sampling of the reset voltages from the sampling of the integrated voltages by using two different channels that are selectively connected to a specific row. Favorable reconsideration is respectfully requested of claim 1.

Although not the same, claim 8 has been amended to recite features similar to amended claim 1. Amended claim 8 is, therefore, not subject to rejection in view of the cited reference, for the same reasons set forth for amended claim 1.

Dependent claims 2-7 depend from amended claim 1, and dependent claims 9-18 depend from amended claim 8. These dependent claims are, therefore, not subject to rejection in view of the cited reference for at least the same reasons set forth for amended claim 1.

Newly Added Claim 19:

Newly added claim 19 further limits claim 1 by reciting the following:

- the succession of reset voltages and the succession of integrated voltages are configured for **simultaneous sampling of the selected row** by the sample-and-hold circuits from the first and second banks, respectively.

Basis for newly added claim 19 may be found, for example, in FIG. 4. As shown, a specific row, for example row-0, includes reset voltages sampled by the first channel, and integrated voltages sampled by the second channel. The sampling of the succession of the reset voltages and the sampling of the succession of integrated voltages for a **selected row** is performed simultaneously by the first and second banks, respectively.

As described above, Gowda does **not** suggest sampling a succession of reset voltages and a succession of integrated voltages by the first and second banks respectively, for a **selected row**.

Favorable consideration is requested for newly added claim 19.

Conclusion

Claims 1-18 and newly added claim 19 are in condition for allowance.

Respectfully submitted,

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